Department of Electronics and Communications
Bharatividyapeeth's College of Engineering
Paschim Vihar, New Delhi

Two week Short Term Course on "Digital Circuit Design and Analysis" (focusing Communication/DSP functionalities)

16-27 July 2018

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Technically sponsored by IEEE India CASS

Objectives and importance of the Event:
The objective of the STC is to train the faculties/researchers/students into the domain of completeness of digital system design with vivado and FPGA implementation. Further aim of the training is to provide capability to integrate the matlab and FPGA for hardware realization of the communication/DSP algorithems/systems. The event further aims to expose the participants to TCL/python scripting skill enabling them to analyze the data with ease .

Importance of the STC:
FPGA is a VLSI based platform for product realization. The product may be varying from different domains. Varying from communication, DSP, Image processing to antenna, microwaves there are uncountable applications. In today's market where time to bring the product in market is very critical FPGA plays a vital role. Also industry is now inclined towards FPGA because of it high perfaming capabilities and less design time.

Similarly knowledge of FPGA is now critical for all faculties for hardware realization of their algorithms as mere matlab simulations could not prove the hardware implementability of the algorithms/systems designed. The completeness of the system become realizable when both matlab and FPGA are interconnected with each other and analyzing the functionality implemented.

Tentative Topics:
Conceptualization, validation, internal verification flows, verticals of FPGA synthesis like ASIC Prototyping, Formal Verification flows , FPGA validation flows , pre silicon validation using FPGA Palladium. Xilinx 7-Series Architecture Overview, Synthesis Technique, Implementation and Static Timing Analysis.

Reprogrammable FPGA. Using the IP Catalog and IP Integrator, Use the IP Catalog to generate a clock resource and instantiate in a design. Use IP Integrate to generate a core and instantiate in the design. Xilinx Design Constraint, Create a project with I/O Planning type, enter pin locations, and export it to the rtl. Then create the timing constraints and perform the timing analysis.

Hardware Debugging. Embedded System Design using Zynq, Zynq Architecture.Extending the Embedded System into Programmable Logic. Adding Peripherals in Programmable Logic. Extend the hardware system by adding AXI peripherals from the IP catalog. Adding Your Own IP Peripheral

Importance and role of Scripting knowledge Tcl / Perl shell/ python for Degital system design and FPGA implementations.

FPGA implementation of any protocols like Ethernet, DDR3 memory, PCI-Express, high speed SERDES protocols, AMBA , USB , HDMI Interconnect(NIC, FlexNoC), Cache Coherency, Protocols like AHB/AMBA,AXI, ACE, OCP, Memory(Flash, SRAM,DDR3/4) and memory controllers. Low power designs, various Clock gating (any 1 or 2 from these protocols)

Communication/DSP system design over FPGA , Antena interface with FPGA, Matlab and FPGA interface procedure and hands on session.
5G Transceivers: Analysis via Hardware Software Co-Design on Zynq SoC
VLSI based reprogrammable digital communication

Registration:

Candidates are requested to deposited/transfer fee to account with details as "State Bank of India" Jwala Heri Paschim Vihar, A/c No: 31976258020, IFSC code: SBIN0006623, micro code: 110002142

Note the transaction number and fill the online form on www.bvcoend.ac.in / or
https://goo.gl/forms/wUPo3aAwjWW2rg543

Registration Fee:

Category	Fees (Rs) (per candidate)
Industry candidate	6000.00
Academia candidate	5000.00
IEEE Member/RF/Student (required to provide letter institution in case of RF/Student)	4000.00
Bulk registration (in case of registration from same institutes is more than 5, required to provide letter from institute)	4000.00

Resource Persons (Confirmed\Invited)

Dr. Arti Noor, Joint Director CDAC Noida
Dr. Sumit J Darak Assistant Professor Indraprastha Institute of Information Technology, Delhi (and Team)
Mr. Kudeep Singh, Guru Jambheshwar University of Science and Technology
Ms. Hitu Sharma, Application Engineer - Signal Processing and FPGA Design, Mathworks India (and team)
Mr. Ankur Sangal, Sr. Application Engineer , CoreEL Technologies
Dr. Manoj Sharma, Associate Prof., Dept. of ECE, BVCOE, New Delhi