BHARATI VIDYAPEETH'S COLLEGE OF ENGINEERING
(Approved by AICTE, New Delhi & Affiliated to Guru Gobind Singh Indraprastha University, Delhi)
(An ISO 9001:2008 Certified Institution)
A-4, Paschim Vihar, Main Rohtak Road, New Delhi-110 063.

Department of Electronics and Communication Engineering

Ref No: BVCOE/ND/ECE/285/25-26

Date: 10/11/25

NOTICE

This is to inform all second year ECE students that under the category of content beyond syllabus for DLCD, a guest Lecture on **"Clocking and its importance in Digital System Design"** has been organized. The **Industry expert** speaker for the session is **Ms. Lalita Gangwar, MJPRU, Bareilly.**

The Lecture will include:

1. Fundamentals of Clock Signals and their role in synchronous digital systems.
2. Clock Distribution, Clock Skew, Jitter, and methods to manage them.
3. Importance of Timing Constraints in FPGA / ASIC Digital System Design.
4. Real-world examples of how proper clocking ensures system reliability and performance.

Request all to seize this opportunity to interact with the expert and elevate your career to new heights.

The details of the same are as follows:

Date: 14th November 2025, Friday.

Time: 10:00 to 11:00 AM

The online link of the session will be shared with the students on official group.

All second year students must attend this session. Attendance is compulsory.

10/11/25

Dr. Neera Agarwal
DLCD Subject Head
ECE Dept

10/11/25

Prof. Kirti Gupta
HOD ECE