BHARATI VIDYAPEETH'S COLLEGE OF ENGINEERING

(Approved by AICTE, New Delhi & Affiliated to Guru Gobind Singh Indraprastha University, Delhi)
(An ISO 9001:2015 Certified Institution)
A-4, Paschim Vihar, Main Rohtak Road, New Delhi – 110 063

Department of Electronics and Communication Engineering

Ref No: BVCOE/ND/ECE/ 630 /25-26

NOTICE

Date: 12th Jan 2026

Subject: Hands-on Training Workshop on FPGA Design Methodology & Smart Camera Applications

Dept of ECE, is organizing a 2-Day Hands-on Training Workshop on FPGA Design Methodology, in collaboration with CoreEL Technologies (India) Private Limited, Bengaluru on 15th -16th Jan 2026. This workshop is designed to provide practical exposure to FPGA design using Xilinx Vivado, ZYNQ architecture, embedded system design, and Python-based productivity tools, along with a Smart Camera application.

Workshop Agenda & Major Topics

Day 1: FPGA Design & Python Productivity

- Overview of FPGA Families
- ZYNQ & ZYNQ MPSoC Architecture
- FPGA Design Flow using Vivado
- RTL Analysis, Synthesis, Implementation & Bitst Generation
- Xilinx Design Constraints (XDC)
- IP Catalog Flow & ILA-based On-chip Debuggin
- Introduction to PYNQ Framework
- Jupyter Notebook Interface
- Python for Data Visualization & Image Processin

Day 2: Embedded Systems & Smart Camera Applic

- ZYNQ-based Embedded System Design
- IP Integrator & AXI-based IP Core Integrat
- Communication between Processing Systen (PS) & Programmable Logic (PL)
- Hardware–Software Co-design using VITIS
- Bitstream & ELF Integration
- Smart Camera Application Development
- MIPI Camera Interface
- Introduction to Visual Recognition Platform

Time and Venue: 10am to 4pm, A405 (ECE Project Lab)

Faculties taking VHDL Programing theory/lab and other interested faculties are requested to attend the same.

Manoj

Dr. Manoj Sharma
Coordinator
Assoc Prof (ECE)

12/1/26.

Prof. Kirti Gupta
HoD (ECE)