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BHARATI VIDYAPEETH'S COLLEGE OF ENGINEERING (Approved by AICTE, New Delbi & Affiliated to Guru Gobbind Singh Indraprastha University, Delbi) (An 180 9001:2015 Certified Institution) A-4, Paschim Vilhar, Main Rolitak Road, New Delbi - 110 063

Beneficiary List (Faculty) 2023-2024

S No	S. No. Name of Faculty		
	· · · · · · · · · · · · · · · · ·	Amount in Rs.	
1	Dr Rekha Bhardwaj	5000	
2	Dr Ashu Soni	5000	
	4250		
4	Anu Yadav	499	
5	Anu Yadav	2000	
6	Rupali Pandey	1950	
7	Dr. P. Trisandhya	500	
8	Dr Rekha Bhardwaj	1950	
9	Dr Kaushal Sharma	850	
10	Dr Sushil Sharma	1493	
11	Dr. Kaushal Sharma	1200	
12	Dr.Nitu	950	
13	Dr Ritika Chauhan	950	
14	Dr Ritika Chauhan	2500	
15	Dr Amit Sharma	5750	
16	Dr Kaushal Sharma	1100	
17	Dr Amrita Pritam	2000	
18	Dr Amrita Pritam	2000	
19	Dr Amrita Pritam	950	
20	Dr Sushil Kumar	1180	
21	Dr Ritika Chauhan	1450	
22	Dr Sushil Kumar	3000	
23	Dr Saurabh Agarwal	5000	
24	Mrs.Ranjana Mishra	10000	
25	Mohit Dayal	1000	
26	Dr.Kaushal Sharma	500	
27	Dr. P.Trisandhya	500	
28	Dr. Charu	500	
29	Ms. Ashima Airan	6000	
30	Dr. Surjit	5117.41	
31	Dr.Jyoti Gupta	4000	
32	Dr.Monica Gupta	8000	
33	Dr. Kirti Gupta	9512	
34	Dr.Monica bhutani	5000	
35	Dr.Monica bhutani	8718	
	Dr. Monica botani	5000	
37	Dr.Mihika Mahindra	3540	
	Dr Yogita Arora	9336	

39	Dr.Saji	0000
40	Dr. Priyanka	8000
41	Ms.Shikha	2080
42	Dr. Kirti Gupta	6000
43	Rachna Narula	8718.54
44	Natasha Rathore	1950
45	Vijay Kumar	1950
46	Dr Deepika Kumar	1950
47	Dr.Priti Nagraj	590
48	Dr. Amrita tikku	1100
49	Dr.Srishti	8500
50	Vijay Kumar	700
51	Rachna Narula	450
52	Dr.Jolly Parikh	450
53	Dr.Jolly Parikh	1000
54	Dr Srishti	4000
55	Ms Rachna	10 000
56	Akanksha	5017
57	Dr.Gargi Mishra	10000
58	Dr. Rakhi	1000
59	Dr. Preet Nagrath	2000
60	Neha Gupta	8300
61		9276
62	Dr.Sarita Yadav	9276
63	Dr. Achin Jain	7000
64	Dr. Arun Kumar Dubey	7000
65	Nisha Malhotra	10000
66	Payal Malik	9294
67	Dr. Mahesh Kumar	1000
68	Neetu Singh	10000
	Dr.Surendra Kaur	8000
69	Dr Shalabh	8260
70	Dr.Sandeep Banerjee	500
71	Dr.Sandeep Sharma	1100
72	Mr. Sandeep Banerjee	1000
73	Dr.Shalabh Mishra	1740
74	Dr Sandeep Sharma	4000
75	Dr. Sangeeta Gupta	500
76	Mr Manish Talwar	500

Total

290446.95

BY COE/R & D/110/23-24

Principal, Broof, Delhi

"五里子

Subject: Res'imbursement of Conference paper fles.

Respected Sir,

I had presented a paper titled "A novel technique for the early diagnosis of Mental Health using Natural Language Processis" in the 7th International conference on Innovative Computing and Communication (I c1cc - 2024), organized by SSCBS, Delli University on 16th February 2024. I had poid amount of RS 10,000 for the Same. Kindly reimburse the conference paper fees.

Your Sincerely,

Dujudi

PR. SKISHTI VASHISHTHA

Assistant Professor

CSE Department

PRINCIPAL
Bharati Vidyapeeth's
College of Engineering
A-4, Paschim Vihar,
New Delhi-63

Jouranded July 24

Revomendend OR Frank Jam 22022 De Sunhi Jam 22022 ICICC-2024



























Springer Springer INTERNATIONAL CONFERENCE ON INNOVATIVE COMPUTING AND COMMUNICATION (ICICC-2024) MTERNATIONAL COMPERENCE ON INNICATIVE oneAPI

Cortificate

This is to certify that Prof. Dr./Mr./Ms. Such to Vashieh Ha

of Mental Health, unerg Natural langs process; in the 7th International Conference on Innovative Computing and Communication (ICICC-2024), organized by Shaheed Sukhdev College of Business

Studies, University of Delhi, New Delhi, India in association with the National Institute of Technology

Patna, India and University of Valladolid, Spain on 16th-17th February 2024.

A-4, Pasch

oonam Verma University of Delhi, Principal, SSCBS New Delhi

Prabhat kumar General Chair

National Institute of Technology,

A.K. Singh

National Institute of Technology, Technical Program Chair Kurukshetra

A Novel technique for the early diagnosis of Mental Health using Natural language processing

Amitkumar Upadhyay¹, Deepika Varshney^{2[0000-0002-9728-0525]} Rishabh³, Srishti Vashishtha^{4[0000-0002-6281-5745]}, Dhruv Jain⁵, Jaishree Meena⁶ and Ashish Khanna⁷

1-3,5 Jaypee Institute of Information Technology, Noida-62, Uttar Pradesh, India

⁴ Bharati Vidyapeeth's College of Engineering, GGSIPU, Delhi, India
 ⁶ Department of Biological Science, Amity University Punjab, Mohali

⁷ Maharaja Agrasen Institute of Technology, GGSIPU, Delhi, India
⁷Center for global health research, Saveetha medical college, Saveetha Institute of medical and Technical sciences, India

4srishtidtu@gmail.com

Abstract. In this work, we delve into the critical issue of mental health, particularly focusing on depression, a condition affecting over 264 million individuals of all ages globally, as reported by the World Health Organization (WHO). The pervasive nature of depression establishes it as a leading cause of disability on a worldwide scale. Recognizing the immense impact of mental health disorders, our research is centered around the imperative of early diagnosis as a crucial preventive measure to address this global concern. At the intersection of linguistics, Artificial Intelligence (AI), and computer science, Natural Language Processing (NLP) emerges as a pivotal field. Our study seeks to leverage NLP in addressing the challenges associated with the early diagnosis of mental health issues. NLP is fundamentally concerned with enabling computers to interpret, analyze, and approximate human speech, offering a sophisticated avenue for understanding the nuances present in mental health-related text data. To contextualize the practical applications of NLP in mental health, we draw attention to the emergence of chatbots such as Woebot, Wysa. Joyable, and Talkspace. These chatbots, available as Android/iOS apps or websites, have the capacity to perform mental health assessments using natural conversation. By integrating NLP techniques, these chatbots exemplify the potential for technology to contribute to mental health assessments in an accessible and user-friendly manner. In summary, our research paper aims to contribute to the intersection of mental health and technology, emphasizing the significance of early diagnosis using NLP techniques.

Keywords: Mental Health, Natural Language Processing, LSTM, Word Embeddings, Artificial Intelligence.



Dr. Srishti Vashishtha <srishti22.v@gmail.com>

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BHARATI VIDYAPEETH'S COLLEGE OF ENGINEERING, **NEW DELHI**

Doc. No.: BV/FRADM/035

Issue No.: 02

Date of Issue: Ist Jan. 2011

ON DUTY LEAVE FORM

It is requested	l that		
I (Name)		LI.	
Name Dr.	South Vashull	tua	
Designation	South Vashish	Deptt. CSE	
may kindly be	e granted Duty leave on th	he dates for the purpose	mentioned below:
Dates	Nature of Work	Venue of Work	Supporting Document"
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	fill (a) or (b) above which		
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	Duty Leave		from sanctioned Anotapeeth's
sancti	•		College of Engineerin
Date:		Signature of P	rincipal Winam Palhi 63
Attach Separa	ate Document Sheet if N	ecessary	



Srishti Vashishtha <srishtidtu@gmail.com>

ICICC 2024: Final Presentation Schedule for Paper ID 786

1 message

ICICC 2024 <icicc.ui@gmail.com> To: Srishtidtu <srishtidtu@gmail.com> Thu, Feb 1, 2024 at 9:55 PM

Dear Author,

Greetings from ICICC 2024!

ICICC-2024 will be organized in Hybrid Mode.

For the paper id , the presentations which have opted ONLINE will be conducted online via ZOOM platform.

For the paper id which has opted offline needs to be present on 16th February 2024 at SHAHEED SUKHDEV COLLEGE OF BUSINESS STUDIES, Dr. K.N. Katju Marg Rohini, Sector 16, PSP Area IV, New Delhi, Delhi -110089 at 9:00 AM sharp.

Please note the following Instructions (ONLINE MODE):

1. You are advised to install ZOOM on your desktop/laptop and rename your profile name as session number-paperid.

For example if your paper id is 113 & session number is S5 then you should rename it as S5-113.

- 2. Only one author will be allowed to present the paper in the session. It may be any author.
- 3. The e-certificates will be sent to all the authors via email latest by 5th March 2024. (Certificates will not be issued to those who failed to attend the event)
- 4. Carefully note your session number and the date of presentation by seeing the schedule attached
- 5. It is mandatory to attend the event for the FULL day on your presentation day (Including Inauguration, Keynotes and Your Session).
- 6. The timings for 16th February 2024 is 9:00 A.M. to 4:00 P.M.

Joining/Meeting link for 16th February 2024 will be shared soon

The timings for 17th February 2024 will be 10:30 A.M. to 4:30P.M.

Joining/Meeting link for 17th February 2024 will be shared soon

Bharati Vidyapeeth's College of Engineering

7. Please prepare your presentation as per the template sent and also attached for both of the & online mode.

8. You will get 8-minutes to present your paper and 2-mins for Q/A session.

https://mail.google.com/mail/u/1/?ik=34566b33cd&view=pt&search=all&permthid=thread-f:1789714495889554079&simpl=msg-f:17897144958895540...











ICICC-2024

INTERNATIONAL CONFERENCE ON INNOVATIVE COMPUTING AND COMMUNICATIONS

Web: icicc-conf.com, Email: icicc.ui@gmail.com

Presentation Schedule of paper selected in SPRINGER in OFFLINE / MODE on 16/02/2024

S.No	Category	Session Number	PAPER IDs
1		SESSION NUMBER-01	43, 53, 73, 87, 93,107
2	Springer	SESSION NUMBER-02	150, 155, 165, 168, 207, 271
3	Spi	SESSION NUMBER-03	291, 292, 307, 326, 335 PRINCIPAL
			Bharati Vidyapeeth's College of Engineering A-4, Paschim Vihar, New Delhi-63

BV/COE/R & D/114/23-24

Date: 01/03/2024

To

(Through proper channel)

BVCOE,

New Delhi

The Principal,

Subject: Request for reimbursement of Rs 3540/- paid for attending One Week Short Term Course and Training Program on VLSI Design organized at National Institute of Electronics and Information Technology, Center of Excellence in Chip Design, Noida.

Respected Sir,

With due respect wish to inform that National Institute of Electronics and Information Technology, Center of Excellence in Chip Design, Noida had organized One Week Short Term Course and Training Program on VLSI Design from 26th to 30th Dec 2023. I have completed the FDP, and for the same I had to remit a fee of Rs. 3540/-. As a dedicated member of the BVCOE faculty, I believe that the dissemination of faculty upgradation contributes to the academic reputation of our institution

I have attached the receipts of the fee submitted, and certificate of the STC along with this application for your kind perusal.

Thanking you in anticipation of affirmative action.

Yours Sincerely,

Mihika Mahendra Assistant Professor

ECE Dept.

BVCOE New Delhi

- Forward at

Reasonage Enrange

National Institute of Electronics & Information Technology, Gorakhpu

(Under Ministry of Electronics & Information Technology, Government of India)
MMM University of Technology Campus, Gorakhpur-273010
[Official Website - https://www.nielit.gov.in/gorakhpur]
Payment E-Receipt

Student's Name	Mihika Mahendra			
Father's Name	Mahesh Mahendra			
Course Name	One Week Short Term Course and Training Program on VLSI Design [26-Dec-20			
Amount Paid (In Rs.)	3540.00 * [Course Fees]			
Course Fee (In Rs.)	3540.00	3540.00		
Reference No. (NIELIT)	NGKP231220115994595 Transaction No.(PayU): 18781849178			
Transaction Date/Time	2023-12-20 16:43:09			
Payment Mode	cc			
Bank Reference No.	335416431805			
PayU Id	18781849178			
PAN No. (NIELIT)	AAATD0315M			
GST No. (NIELIT)	09AAATD0315M2ZU			
	*** Payment Verif	ed at NIELIT ***		

^{*} Fee inclusive of GST

For Accounts Section Use Only

Verified By (NIELIT): Sh. Nikhil Kumar Chaurasiya, Assistant (Accounts)

Date: 21-Dec-2023

***** This is system generated receipt, Hence no signature is required. *****

राष्ट्रीय इलेक्ट्रॉविकी एवं सूचना श्रीहोगिकी संस्थान (रा.इ.सू.प्रौ.सं)

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

क्षात्रक अध्यक्षकारक स्वतंत्रक विकास का प्रकारक पहुलेक्ट्रोनिकी <mark>ओरस्स्चना प्रोह्मोगिकी संत्रालय; भारत सरकार</mark>

Ministry of Electronics & Information Technology (Meity), Govt. of India



Certificate No.: NIELIT/NOI/003

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CHEANINGS STREET

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नाम Name	: MIHIKA MAHENDRA
भाता का नाम Mother's Name	ARUNA MAHENDRA
पिता का नाम Father's Name	, MAHESH MAHENDRA
रजिस्ट्रेशन संख्या Registration No.	: NIELIT/GKP/IC/A11/11599
ONE WEEK SHORT TERM COURS of 01 WEEK / 40 HOUR(S)	nentioned candidate has successfully completed a course of EAND TRAINING PROGRAM ON VLSI DESIGN duration from 26.12.2023 to 30.12.2023 te of Electronics and Information Technology (NIELIT IN-CAMPUS mode with S grade.
FPGAs: Types, Architecture, Applica	Curriculum of the Course Ition; Synthesizing a RTL Design on FPGA, ASIC Design Flow, RTL FT (Design for testability, Physical Design.
श्रेणियों का आख्यान 8 GRADE LEGENDS	0% and above 70% to <80% 60% to <70% 50% to <60% एस S ए A बी B सी C
Program Coordinator Issued Date: 20.02.2024	Digitally signed by Dharmendra Mishra Kumar Mishra Date: 2024.02.29 12:12:31 +05'30' Director College of Engineering

A-4, Paschim Vihar, New Delhi-63

PS-1D, Behind Brahampurtra Shopping Complex, Sector 29, Noida, UP - 201303

Head Quarter

National Institute of Electronics & Information Technology

NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8, Dwarka, New Delhi - 110077

National Institute of Electronics & Information Technology, CoE Noida



BHARATI VIDYAPEETH'S COLLEGE OF ENGINEERING, **NEW DELHI**

Doc. No.: BV/FRADM/035

Issue No.: 02

Date of Issue: Ist Jan. 2011

ON DUTY LEAVE FORM

It is requested	d that		
I (Name)		, a	
	. MIHIKA	- 74.	
Designation	ASTT. PROPESSOR	Deptt. ECF	
	e granted Duty leave on th		e mentioned below:
Dates	Nature of Work	Venue of Work	Supporting Document*
26/12/23 to 29/12/23	FDP at NIELLT, NOIDA	NOIDA	Attached
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<i>(</i> 1)	Name		Signature
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Attach Sanara	te Document Sheet if Neo		New Delhi-63



National Institute of Electronics and Information Technology, NOIDA

Name of Group: Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

Name of Course: One-week Short Term Course & Training Program on VLSI Design

Objective: The one-week VLSI course aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing. Participants will gain hands-on experience with Cadence EDA toolsuite, explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered 30+ chip tapeouts for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Duration: 5 Days (40 Hours)

NOTE: Only in physical mode. Limited seats (Only 20)

<u>Eligibility:</u> Students who have completed or pursuing B.E. / B.Tech. / M.E / M.Tech. **Note:** Research Scholars, Faculty members and Industry professionals can also enrol **Prerequisites:** -

1. Basic knowledge of digital circuits and logic gates.

2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL

3. Familiarity with a Unix/Linux environment and command-line interface

Course Fees: Rs. 3,540/- (incl. GST)

Course Date: 26 December 2023 to 30 December 2023

Registration Process: Candidates have to apply in prescribed application form through online registration portal https://regn.nielitvte.edu.in/ or through Android App "NIELIT Kaushal Setu". The duly filled form along with the course fees Rs. 3,540/- (incl. GST) has to be submitted in online mode through the above link. The Fees deposited is Non-Refundable.

Course Content:

Day 1		
1 st Half	Inauguration & Invited talk	
1 st Half	FPGAs: Types, Architecture, Application	IS to a real appropriate the second s
2 nd Half	FPGAs: Hands on Session 1. HDL Design, Simulation 2. Dumping Code into FPGA 3. Hardware Debugging 4. Mark Debug Feature 5. Integrated Logic Analyzer (ILA) core	PRINCIPAL Bharati Vidyapecth's College of Engine. 18
Day 2		A-4, Paschim Vil

Partha P. Adhikari,

Additional Director/Scientist 'E' & OIC, CoE Chip Design Noida Centre PRASHANT PAL (Scientist-C)



National Institute of Electronics and Information Technology, NOIDA

l st Half	Synthesizing RTL Design on FPGA: Lecture, Demonstration, Lab session Hands on Session 1. FPGA based Synthesis, Design and Implementation 2. Implementation and Static Timing Analysis		
2 nd Half			
Day 3	L' la coolon		
1 st Half	ASIC Design Flow: Lecture, Demonstration, Lab session 1. Semi-custom Design Flow 2. Full-custom Design Flow 3. IP Development		
2 nd Half	RTL Design & Verification: Lecture, Demonstration, Lab session 1. Overview of RTL Integration 2. RTL Linting Concepts 3. Clock Domain Crossing Concepts 4. SoC Methodology & IP Integration 5. System Verilog 6. UVM, OVM, System C 7. Verification IPs		
Day 4	The state of the s		
1 st Half	Synthesis: Lecture, Demonstration, Lab Session 1. Compilation 2. Elaboration 3. Various Synthesis Optimization Techniques 4. Low Power Features (IEEE 1801-2018) 5. Physical Aware Synthesis Flow 6. Optimization wrt Area & Timing Concepts 7. Synthesis Output: Netlist, Abstract Models, Hard Macros etc. 8. Unified Power Format (UPF), Logical equivalence Check Concepts		
2 nd Half	DFT (Design for Testability): Lecture, Demonstration, Lab Session 1. Basics of DFT 2. Test Architecture 3. Scan Chain Insertion, Compression Insertion 4. Clock & Reset Controllability 5. ATPG 6. JTAG, Boundry Scan 7. MBIST/LBIST		
Day 5			
1st Half	DFT Lab Session Contd		
2 nd Half	Physical Design: Lecture, Demonstration, Lab Session PRINCIPAL 1. Floorplan, Placement, Routing Bharati Vidyapeeth's 2. CTS College of Engineering 3. Multiple Clocks and Exceptions A-4, Paschim Vihar,		
	Q & A New Delhi-63		

Partha P. Adhikari, Additional Director/Scientist 'E' & OIC, CoE Chip Design Noida Centre PRASHANT PAL (Scientist-C)



National Institute of Electronics and Information Technology, NOIDA

* There will be 8 Hours Session per day.

Mode of Payment: Fees can be paid either by debit/credit card or in any online mode. For any queries and more details please contact on 8218724641/9711177638

Course Venue

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahampurtra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

Registration Link: https://regn.nielitvte.edu.in/

or

Through Android App "NIELIT Kaushal Setu"

PRINCIPAL
Bharati Vidyapeeth's
College of Engineering
A-4, Paschim Vihar.
New Delhi-63

Partha P. Adhikari, Additional Director/Scientist 'E' & OIC, CoE Chip Design Noida Centre PRASHANT PAL (Scientist-C)



National Institute of Electronics & Information Technology, Gorakhpur

(Under Ministry of Electronics & Information Technology, Government of India) MMM University of Technology Campus, Gorakhpur-273010
[Official Website - https://www.nielit.gov.in/gorakhpur]

Payment E-Receipt

Student's Name	Mihika Mahendra		
Father's Name	Mahesh Mahendra		
Course Name	One Week Short Term Course and Training Program on VLSI Design [26-Dec-20		
Amount Paid (In Rs.)	3540.00 * [Course Fees]		
Course Fee (In Rs.)	3540.00		
Reference No. (NIELIT)	NGKP231220115994595 Transaction No.(PayU): 18781849178		
Transaction Date/Time	2023-12-20 16:43:09		
Payment Mode	cc		
Bank Reference No.	335416431805		
PayU Id	18781849178		
PAN No. (NIELIT)	AAATD0315M		
GST No. (NIELIT)	09AAATD0315M2ZU		
	*** Payment Ver	ifed at NIELIT ***	

^{*} Fee inclusive of GST

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Date: 21-Dec-2023

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